



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/824,938

04/15/2004

Ludovic Ruat

01RO13054507

7278

27975

7590

05/29/2008

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.  
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE  
P.O. BOX 3791  
ORLANDO, FL 32802-3791

EXAMINER

KANGARLOO, RAMTIN

ART UNIT

PAPER NUMBER

2619

NOTIFICATION DATE

DELIVERY MODE

05/29/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/824,938	<b>Applicant(s)</b> RUAT ET AL.	
	<b>Examiner</b> RAMTIN KANGARLOO	<b>Art Unit</b> 2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 3/31/2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### **Response to Amendment**

1. Applicant's amendment filed on March 31, 2008 has been entered. Claims 1-17 are still pending in this application, with claim 1, 7 and 13 being independent.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Rakib et al. (US Patent Application Publication No.2001/0024474) in view of Douceur (US Patent No. 6067547).

Regarding **Claim 1**, Rakib discloses an asynchronous frame receiver comprising: an input for receiving an asynchronous frame comprising a break character (See Paragraph [0143], lines 1-8 and Fig. 2A, for synchronization frame and break character), and a hot-plugging circuit for connecting to an asynchronous data bus that is operating, said hot-plugging circuit detecting the break character, and leaving an initial idle state and switching to at least one operating mode when the break

Art Unit: 2619

character has been detected (See Page. 21, Paragraph [0241] and Page. 39, Paragraph [0384] and Page. 49, Paragraph [0443]).

Rakib does not disclose the break character comprising at least three bits, each and every bit of the break character having a same value. Douceur teaches the break character comprising at least three bits, each and every bit of the break character having a same value (See col. 16, lines 18-23).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to mount three bits divider taught by Douceur on to the synchronization device as shown in Rakib in order to ensure a better quality of service by reducing packet errors during recovery.

Regarding **Claim 2**, Rakib and Douceur disclose all of the limitations as applied to claim 1. Further Rakib discloses the asynchronous frame further comprises a synchronization character after the break character, the asynchronous frame receiver further comprising: a clock recovery circuit that is activated after receiving the synchronization character at the input after detecting the break character (See Page. 6, Paragraph [0071] and Page. 46, Paragraph [0429] and Page. 46, Paragraph [0431]).

Regarding **Claim 3**, Rakib and Douceur disclose all of the limitations as applied to claim 2. Further Rakib discloses said clock recovery circuit measures a clock period in the synchronization character (See Page. 32, Paragraph [0336]).

Regarding **Claim 4**, Rakib and Douceur disclose all of the limitations as applied to claim 3. Further Rakib discloses said clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character (See Page. 35, Paragraph [0355]).

Regarding **Claim 5**, Rakib and Douceur disclose all of the limitations as applied to claim 1. Further Rakib discloses said hot-plugging circuit comprises a state machine (See Page. 49, Paragraph [0443]).

Regarding **Claim 6**, Rakib and Douceur disclose all of the limitations as applied to claim 1. Further Rakib discloses a substrate; and wherein said hot-plugging circuit is on said substrate so that the asynchronous frame receiver comprises an integrated circuit (See Page. 32, Paragraph [0333]).

Regarding **Claim 7**, Rakib discloses a microcontroller comprising: a universal asynchronous frame receiver transceiver (UART) comprising an input for receiving an asynchronous frame comprising a break character (See Paragraph [0143], lines 1-8 and Fig. 2A, for synchronization frame and break character); and  
a hot-plugging circuit for connecting to an asynchronous data bus that is operating, said hot-plugging circuit detecting the break character, and leaving an initial idle state and switching to at least one operating mode when the break

Art Unit: 2619

character has been detected; and a processor connected to said asynchronous frame receiver (See Page. 21, Paragraph [0241] and Page. 39, Paragraph [0384] and Page. 49, Paragraph [0443] and Fig. 8).

Rakib does not disclose the break character comprising at least three bits, each and every bit of the break character having a same value. Douceur teaches the break character comprising at least three bits, each and every bit of the break character having a same value (See col. 16, lines 18-23).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to mount three bits divider taught by Douceur on to the synchronization device as shown in Rakib in order to ensure a better quality of service by reducing packet errors during recovery.

Regarding **Claim 8**, Rakib and Douceur disclose all of the limitations as applied to claim 7. Further Rakib discloses a memory connected to said processor (See Page. 16, Paragraph [0208]).

Regarding **Claim 9**, Rakib and Douceur disclose all of the limitations as applied to claim 7. Further Rakib discloses the asynchronous frame further comprises a synchronization character after the break character, said UART further comprising: a clock recovery circuit that is activated after receiving the synchronization character at the input after detecting the break character (See Page. 6, Paragraph [0071] and Page. 46, Paragraph [0429] and Page. 46, Paragraph [0431]).

Regarding **Claim 10**, Rakib and Douceur disclose all of the limitations as applied to claim 9. Further Rakib discloses said clock recovery circuit measures a clock period in the synchronization character (See Page. 32, Paragraph [0336]).

Regarding **Claim 11**, Rakib and Douceur disclose all of the limitations as applied to claim 10. Further Rakib discloses said clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character (See Page. 35, Paragraph [0355]).

Regarding **Claim 12**, Rakib and Douceur disclose all of the limitations as applied to claim 7. Further Rakib discloses said hot-plugging circuit comprises a state machine (See Page. 49, Paragraph [0443]).

Regarding **Claim 13**, Rakib discloses a method for connecting an asynchronous frame receiver to an asynchronous data bus that is operating, the method comprising:

setting the asynchronous frame receiver to an initial idle state; receiving at an input of the asynchronous frame receiver an asynchronous frame comprising a break character (See Paragraph [0143], lines 1-8 and Fig. 2A, for synchronization frame and break character), and detecting the break character and switching the asynchronous frame receiver from the initial idle state to at

Art Unit: 2619

least one operating mode (See Page. 21, Paragraph [0241] and Page. 39, Paragraph [0384] and Page. 49, Paragraph [0443]).

Rakib does not disclose the break character comprising at least three bits, each and every bit of the break character having a same value. Douceur teaches the break character comprising at least three bits, each and every bit of the break character having a same value (See col. 16, lines 18-23).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to mount three bits divider taught by Douceur on to the synchronization device as shown in Rakib in order to ensure a better quality of service by reducing packet errors during recovery.

Regarding **Claim 14**, Rakib and Douceur disclose all of the limitations as applied to claim 13. Further Rakib discloses at least one operating mode comprises a read mode (See Page. 4, Paragraph [0025]).

Regarding **Claim 15**, Rakib and Douceur disclose all of the limitations as applied to claim 13. Further Rakib discloses the asynchronous frame further comprises a synchronization character after the break character; and further comprising activating a clock recovery circuit after receiving the synchronization character at the input after detecting the break character (See Page. 6, Paragraph [0071] and Page. 46, Paragraph [0429] and Page. 46, Paragraph [0431]).



Regarding **Claim 16** Rakib and Douceur disclose all of the limitations as applied to claim 15. Further Rakib discloses the clock recovery circuit measures a clock period in the synchronization character (See Page. 32, Paragraph [0336]).

Regarding **Claim 17**, Rakib and Douceur disclose all of the limitations as applied to claim 1. Further Rakib discloses the clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character (See Page. 35, Paragraph [0355]).

### **Response to Amendment**

1. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

Art Unit: 2619

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAMTIN KANGARLOO whose telephone number is (571)270-3452. The examiner can normally be reached on Mon to Fri 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chirag Shah can be reached on (571) 272- 3144. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit: 2619

/RAMTIN KANGARLOO/

Examiner, Art Unit 2619

April 25, 2008

/Chirag G Shah/

Supervisory Patent Examiner, Art Unit 2619